Multiple Nanowire Gate Field Effect Transistors

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Abstract

Novel metal oxide semiconductor field effect transistor (MOSFET) architectures aimed at sub 1V operation with enhanced current driving capability are reported. In our design, the planar channel region in a conventional MOSFET is replaced by an array of isolated Si wires. Directional metal coverage of the two sidewalls and the top surface of each Si wire help achieve enhanced gate control. Sub 1V operation is achieved by reducing cross-sectional wire diameters to ~0.05 μm. Since the conventional optical lithography techniques lack patterning resolution at this scale, a mix and match approach with interferometric lithography was employed. Super-resolution capability of interferometric lithography was applied to pattern nanoscale Si wires, while optical lithography was used to pattern non-critical device levels. Drain current versus gate voltage measurements of planar and wire MOSFETs demonstrated the superiority of the multiple nanowire gate design. Increasing the number of 0.05-μm diameter wires significantly increased current flow in the channel region without sacrificing the low-voltage operation. The mix and match approach for patterning critical level nanoscale features represents a low-cost complement to optical lithography.

1. Introduction

Silicon metal oxide semiconductor field effect transistor (MOSFET) is the most dominant electronic device in integrated circuit manufacturing [1]. In a MOSFET, the gate as the controlling element is electrically isolated from the channel region by a thin oxide film. The switching action by the gate is used as the building block for microprocessors and memory chips. The consumer requirements for faster, low-power, inexpensive computers have stimulated both the advanced semiconductor device research, and the development of cost-effective manufacturing Technologies [2]. This trend has been strongly reinforced by recent shifts toward multi-media and networking applications requiring increasingly higher memory devices for image data recording and analysis [3]. Since Si MOSFETs have been the mainstay of IC manufacturing over the last two decades, extensive research has focused on these devices aimed at reduced operating voltage, and increased speed and packing densities [4-5]. In order to achieve sub 1V operations, most researchers have relied either on thin (~0.1 μm) Si films in SOI configuration [6], or on extremely thin (~0.01 μm) junctions in bulk Si [7]. Most of these device designs take advantage of ion-implantation technology, improved threshold control of heavily doping channels, and heavily-doped poly Si over extremely thin (~0.002-0.005 μm) thermally grown gate oxide. Typically, gate lengths are ~0.15-0.1 μm, and widths ~3-10 μm. Several novel MOSFET designs have also been investigated including vertical [8-9], and gate all around (GAA) device configurations [10-11].

2. Interferometric Lithography for Nanoscale Fabrication

For the last thirty years, the semiconductor industry has followed Moore's law, which predicts a doubling of transistor performance and density every 18 months [12]. Advances in optical lithography have been responsible for much of this extraordinary progress. Continued improvements in resolution are facing serious technical challenges primarily because of the fundamental optical lithography diffraction limits. Optical resolution enhancement techniques (RETs), including off-axis illumination [13], phase-shift masks [14], and optical proximity correction [15] have been developed to meet higher resolution requirements. Optical RETs can provide ~10-20 % resolution improvement of the critical dimension (CD) at the cost of increasing process and mask complexity [16]. For sub 0.1-μm CDs, post optical lithography techniques, including x-ray [17], e-beam [18], projection ion-beam and EUV [19] are expected to play a major role. These techniques possess the requisite resolution, however, their integration into the semiconductor-manufacturing environment will require extensive infrastructure development due to their incompatibility with the existing optical manufacturing technological base.

We have developed interferometric lithography (IL) techniques as an alternative for printing sub 0.1-μm features. In its simplest version, IL is an interference between two coherent waves resulting in a 1-D periodic pattern defined by $\lambda/2\sin\theta$, where λ is the wavelength, and 2θ is the angle between two beams [20]. Thus, for exposure with an Ar-ion laser at λ=0.36 μm, θ=60°, d ~0.2 μm, CDs ~0.05-0.1 μm (CDs ~d/2-d/4) can be easily achieved in commercially

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14. ABSTRACT

Novel metal oxide semiconductor field effect transistor (MOSFET) architectures aimed at sub 1 V operation with enhanced current driving capability are reported. In our design, the planar channel region in a conventional MOSFET is replaced by an array of isolated Si wires. Directional metal coverage of the two sidewalls and the top surface of each Si wire help achieve enhanced gate control. Sub 1 V operation is achieved by reducing cross-sectional wire diameters to ~0.05 mu m. Since the conventional optical lithography techniques lack patterning resolution at this scale, a mix and match approach with interferometric lithography was employed. Super-resolution capability of interferometric lithography was applied to pattern nanoscale Si wires, while optical lithography was used to pattern non-critical device levels. Drain current versus gate voltage measurements of planar and wire MOSFETs demonstrated the superiority of the multiple nanowire gate design. Increasing the number of 0.05 mu m diameter wires significantly increased current flow in the channel region without sacrificing the low-voltage operation. The mix and match approach for patterning critical level nanoscale features represents a low-cost complement to optical lightography.

15. SUBJECT TERMS

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available I-line photoresist. Since there is no z-dependence to an IL exposure pattern, DOF is essentially infinite, and limited by laser coherence length and beam overlaps. IL was used in developing an exposure tool used at SEMATECH for fabrication of nanoscale test patterns [21]. Using multiple exposures either in the same photoresist level, or in multiple levels, a wide variety of complex 1-D and 2-D structures can be synthesized [22]. Recently, we have demonstrated a mix and match approach of interferometric and optical lithographies to print a critical feature of an electrical test pattern [23]. Finally, we have also developed nonlinear spatial period division techniques that have the potential to extend IL beyond its theoretical $\lambda/2$ limit [24]. In a typical interferometric lithography process, grating patterns are first formed in photoresist followed by a pattern transfer to the underlying substrate [25]. Using wet, or dry etching techniques, the photoresist patterns can be transferred into Si substrates as shown in Figure 1 by two examples of 0.05-0.1-μm linewidth 1-D gratings wet-etched in (110) Si [26]. The grating structures in Fig. 1 demonstrate both the resolution and fine-line patterning capability of IL.

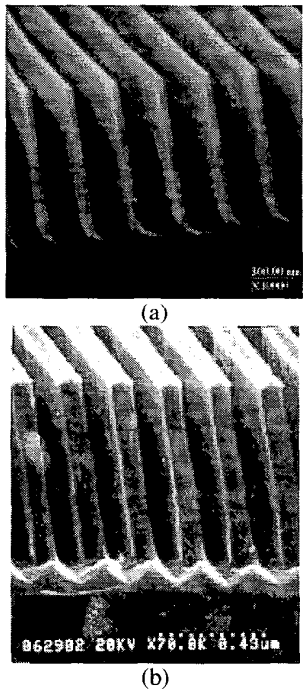


Figure 1 SEM pictures of 0.05-μm linewidth structure at 0.3-μm period (a), and 0.1-μm linewidth structure at 0.2-μm period (b), depth is ~1.0 μm for both gratings.

2.a Mix and Match Approach for MOSFET Fabrication

Interferometric lithography inherently prints periodic structures, therefore, it can be gainfully employed as a complement to optical lithography in a mix and match scheme in which IL provides the high-resolution features, and OL provides the arbitrary patterning capability required for complete devices and circuits. This can potentially lead to industrial application of IL in printing critical features such as transistor gates or vias that are largely periodic in nature, while the OL is used to define remaining transistor and interconnect geometries. Similar mix & match approaches have been reported for x-ray [17] and e-beam lithographies [18].

In order to fabricate MOSFETs, a photomask set was designed. Critical features of the photomask set were separate channel regions to accommodate wire length and density variations. Interferometric lithography was employed for patterning wires in the channel regions. Source, drain and gate regions were defined by optical lithography. All devices were fabricated on a p-type (8-16 Ω-cm) 0.2-μm thick Si film in SOI configuration. The processing for both planar and wire MOSFETs was identical except for the IL step in wire fabrication. For most of the devices reported here, a thick (~0.06 μm) gate oxide grown in O_2 ambient was used. Source and drain region n-type diffusion was obtained with a spin-on phosphorous diffusion source (P-8545). Ohmic contacts were formed by annealing e-beam evaporated Al film at ~450 °C in forming gas for ~15 minutes. Reactive ion etching to form isolated Si wires was carried out using a Technics, West parallel-plate reactor (PEII-A) in $CHF_3/O_2/SF_6$ plasma chemistry.

Figure 2 shows SEM pictures of the planar and single wire MOSFET devices. The planar region had a width of 3.0 μm, and its length was varied from ~2-10 μm. The diameter of the Si wire shown in Fig. 2 is ~0.25 μm. Figure 3 shows MOSFETs fabricated with two and four wires in the channel region. In all cases, planar devices were fabricated side-by-side on the same chip to provide a relative performance comparison with respect to wire devices. For wire MOSFETs reported here, lengths were varied from 2-10 μm, with wire diameters from ~0.25 μm to ~0.05 μm. From the I-V measurements in the section below, it will be demonstrated that as the wire cross-sectional diameters approach ~0.05 μm, MOSFET turn-on voltage drops to ≤ 1 V.

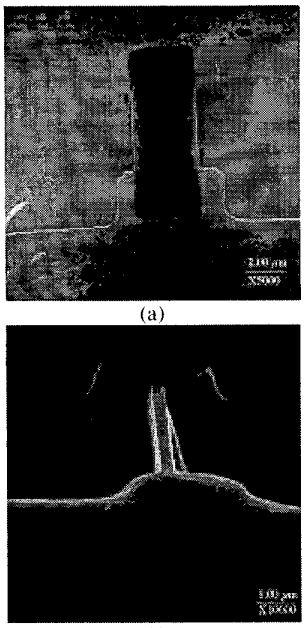


Figure 2 SEM picture of a planar 3.0-μm wide Si channel (a) formed by OL exposure, and a 0.25-μm wide Si channel (b) using mix and match approach. OL was used to define the contacts and planar channel, IL was used to define the 0.25-μm wide line.

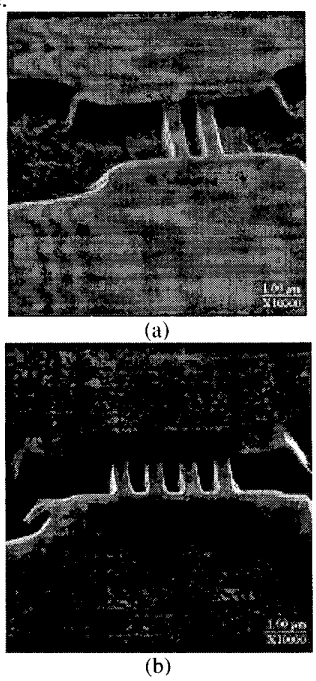


Figure 3 Two (a) and four (b) channel MOSFETs fabricated using mix and match approach, the channel separation is ~0.8 μm, and width ~0.25 μm.

3. I-V Characterization of Wire MOSFETS

All the I-V measurements were carried out using a Tektronix 370 curve tracer. Figure 4 shows typical I-V measurements from the planar and wire devices. It is seen that both these devices operate in the depletion mode; the planar devices have a non-saturation behavior with no channel inversion. The wire MOSFETs show near-ideal saturation current response combined with complete channel inversion. The current in the wire MOSFETs is ~15 times less than the planar devices, presumably due to less Si volume. As we reduce the wire cross-sections, we see turn-on at lower voltages. Figure 5 shows the I-V response from a single channel MOSFET with ~0.1-μm channel diameter. It is seen that the drain current saturation is reached for ~1 V in both cases; the hysteresis in measurements is due to the lack of resolution of the Tektronix curve tracer, and can be resolved by improved data acquisition setup. Figure 5 shows that the channel inversion takes place for gate voltages ~-1 V to ~-1.5 V. Using a simple test circuit, we measured I_d variation as a function of gate voltage as shown in Fig. 6. It is seen that for the 0.1-μm device, the sub-threshold slope is ~100 mV/decade, and V_t is ~-1.7 V. This measurement was carried out on the device with I_d versus V_d characteristics shown in Fig. 5 (a). In comparison, the planar device sub-threshold is very large, and current cannot be turned off as seen below in Fig. 4 (left). Considering that the gate oxide thickness for the 0.1-μm devices is ~0.06 μm, the wire MOSFET performance is remarkable. These results also demonstrate that narrow channels provide better control over the channel potential. Another advantage is enhanced gate control from the top and sides in contrast to the topside in conventional planar transistors [28]. Theoretical simulations using DEVICE 3D software from Silvaco International Inc. [18] also predict large current per unit width as channel width is reduced below 0.1 μm.

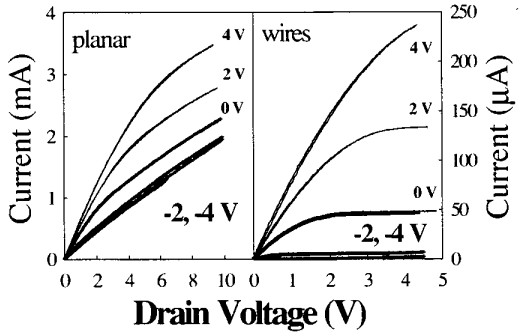
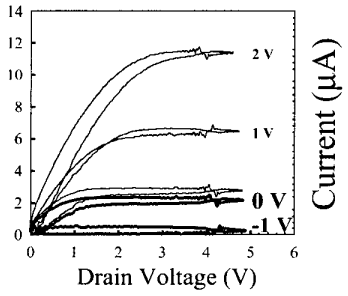
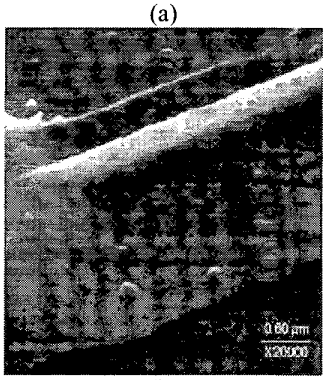


Figure 4 I-V measurements from planar (left) and multiple wire (right) Si MOSFETs.

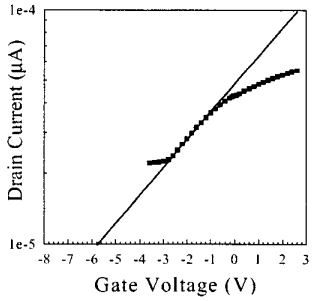


(a)



(b)

Figure 5 I-V measurements from a single channel 1V MOSFET (a) and its SEM picture (b).



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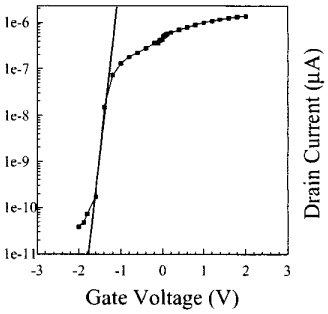


(b)

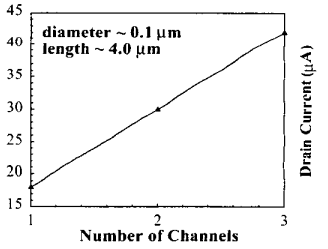
Figure 6 I_d versus V_g measurements for planar (a), and 0.1-μm wire (b) MOSFET devices at V_{ds}=0.1 V.

3.a MOSFET Performance with Wire Density

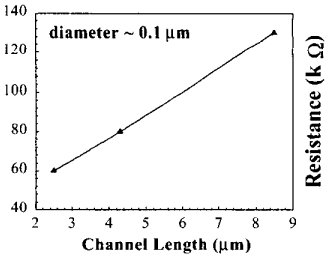
Superior performance of wire configuration over planar has been demonstrated in Figs. 4-5. At nanoscale dimensions, the current carrying capacity is significantly reduced. Therefore, it is important to characterize the device response as the number of wire channels is increased. Some general trends can be plotted for the nanoscale gate channel MOSFETs. Figure 7 (a) shows the linear response of the drain current as a function of the number of wires for ~0.1-μm diameter wires. Figure 7 (b) shows resistance variation for a single-wire channel as a function of its length. It is seen that resistance increases linearly with length as expected from a simple length dependence of a resistor.

3.b Sub 1V MOSFETS

As active gate-channel cross-sectional dimensions are reduced to ≤ 0.05 μm, even lower voltage transistor operation in comparison with earlier measurements (Fig. 5) are observed. At these extreme nanoscale dimensions, the current carrying capacity was reduced to ~1-2 μA, which is in good agreement with similar



(a)

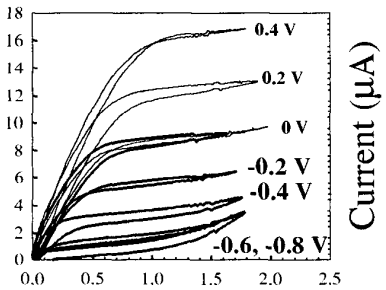


(b)

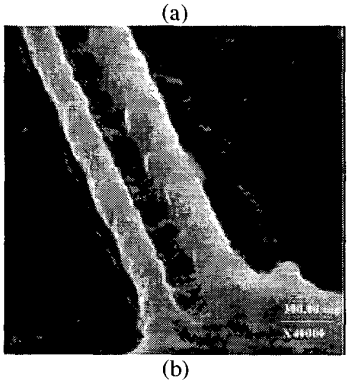
Figure 7 Drain current variation with number of channels (a), and resistance variation of a single channel with length (b).

devices reported in literature. By increasing the number of 0.05-μm channels, the channel current can be enhanced, while still maintaining the low-voltage operation. By reducing wire-channel spacing, the same photo mask set was used for fabrication of multiple ~0.05-μm diameter channel MOSFETs. Figure 8 (a) shows the I-V measurements from a two wire-channel MOSFET, the length of the wires was ~3.0 μm, and the estimated diameter ~0.05 μm.

The I-V measurements in Fig. 8(b) demonstrate that the saturation current is achieved at < 1 V. The saturation current at 8 μA is at least 4-8 times higher than that observed for single-channel MOSFETs operating at the same low-voltages. The saturation current shows a small positive slope as a function of the drain voltage. For reversed gate polarity, channel current is reduced to < 1 μA at -0.8V gate voltage. We should point out that in all the devices reported here, only the transverse gate dimension has been reduced to ~0.05-μm dimensions. A second device parameter, which is of importance with respect to switching speed and short channel effects, is the longitudinal gate length. Using a second IL step, gate lengths can also be reduced to ~0.5-0.1 μm range.



(a)



(b)

Figure 8 I-V Measurements from a 2 wire-channel transistor (a), and the SEM picture of the channel region (b).

4. Summary And Future Work

A mix and match lithography approach to fabricate low-voltage MOSFETs was developed. In the new MOSFET architecture a conventional planar channel region is replaced by individually isolated, sub 0.1-μm channels formed in a gate all around configuration to provide enhanced control. Enhanced gate control in comparison with a planar device was experimentally demonstrated by I_d versus V_g measurements in Fig. 6. The low turn-on voltage was realized for cross-sectional channel dimensions of ~0.05 μm. By increasing the channel density, higher current through the channel regions was conducted without sacrificing the low-voltage operation as shown in Fig. 8. The mix & match lithography approach employed here is inexpensive, applicable over large areas, and compatible with existing semiconductor manufacturing environment. However, in order to realize the full potential of this technology, optimization with respect to several device parameters is require. Some parameters are listed below.

i. Gate oxide quality & thickness,
ii. Poly-Si gate,
iii. Doping variation in the source, drain, and channel regions,
iv. Surface damage assessment during reactive ion etching,
v. Variation in the number of gate channels and diameters,
vi. CMOS process compatibility, i.e., p- and n-channel MOSFETs characterization, and
vii. Statistical evaluation of the mix & match approach over for manufacturing applications.

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